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09/871,159	05/31/2001	David R. Evoy	VLSI.300PA	7445

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
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8

Please find below and/or attached an Office communication concerning this application or proceeding.

PLG

Office Action Summary	Application No. 09/871,159	Applicant(s) EVOY ET AL.	
	Examiner Suresh K Suryawanshi	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "270" at page 9, lines 17-18. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: patent application numbers are not provided on page 1, lines 3-8.

Appropriate correction is required.

4. The disclosure is objected to because of the following informalities: brief description of drawings need to be corrected to reflect the submitted formal drawings, paper no. 4, accordingly as there are 6 sheets of drawings labeled as Fig. 1-1, Fig. 1-2, Fig. 1-3, Fig. 1-4, Fig. 2-1, and Fig. 2-2.

Appropriate correction is required.

5. The disclosure is objected to because of the following informalities: patent application number is not provided on page 5, line 29.

Appropriate correction is required.

6. The disclosure is objected to because of the following informalities: patent application number is not provided on page 5, line 29.

Appropriate correction is required.

7. The disclosure is objected to because of the following informalities: label "FIG. 1" is not in any sheet of drawings (page 7, line 11; page 8, line 30).

Appropriate correction is required.

8. The disclosure is objected to because of the following informalities: label "FIG. 2" is not in any sheet of drawings (page 8, line 29; page 9, line 17, 28; page 10, line 28).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-14 and 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Cassiday et al (US Patent no 5,978,419).

11. As per claim 1, Cassiday et al teach

a parallel bus having parallel bus lines adapted to transfer digital data, the parallel bus lines being arranged in a plurality of groups wherein each group includes a plurality of data carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried over the plurality of data-carrying lines of the group [Fig. 1; col. 3, lines 45-63];

a first module adapted to transfer sets of data concurrently on the plurality of groups of lines of the parallel bus [Fig. 1; col. 3, lines 45-63; col. 6, lines 47-50; transmitter module]; and

a second module adapted to collect, for each group, the digital data carried from the first module over the plurality of data-carrying lines as synchronized by the clock signal for the group and adapted to align the data collected for each group and overcome any skew-caused misalignment between data concurrently transferred in different groups [Fig. 1; col. 3, lines 45-50; col. 4, lines 1-10, 25-27, 33-37; receiver module].

12. As per claim 2, Cassiday et al teach that for each group the clock path is implemented using a pair of the parallel bus lines [Fig. 1; col. 8, lines 13-14; differential signal wires LINK(1) and LINK(0) connecting each transmitter circuit to each receiver circuit].

13. As per claim 3, Cassiday et al teach that for each group, data carried by the plurality of data-carrying lines are synchronized by the differential clock signal to tolerate any skew-caused misalignments between data concurrently transferred in the group [Fig. 1; col. 8, lines 13-14; differential signal].

14. As per claim 4, Cassiday et al teach that for each group, data carried by the plurality of data-carrying lines are synchronized by the clock signal [Fig. 1; col. 3, lines 45-63; col. 4, lines 1-10, 25-27, 33-37].

15. As per claim 5, Cassiday et al teach that the clock signal is a differential clock signal [Fig. 1; col. 8, lines 13-14; differential signal wires LINK(1) and LINK(0) connecting each transmitter circuit to each receiver circuit].

16. As per claim 6, Cassiday et al teach that the first and second modules are further adapted to process concurrent data [Fig. 1; col. 6, lines 47-48].

17. As per claim 7, Cassiday et al teach that the data carried over the plurality of data carrying-lines is encoded [Fig. 1; inherent to the transmitter], and wherein the second module includes for each group: a receiver circuit responsive to the clock signal and adapted to receive the digital data carried from the first module over the plurality of data-carrying lines [Fig. 1], a data decoder adapted to decode the received digital data [Fig. 1; inherent to the receiver]; and a

FIFO buffer adapted for storing the decoded data [Fig. 4; RCV BUFFER 82; col. 11, line 17; a receive buffer circuit 82].

18. As per claim 8, Cassiday et al teach that for each group, the data decoder converts an X-bit value to a Y-bit value [inherent to the characteristic of a decoder].

19. As per claim 9, Cassiday et al teach that for each group, the clock signal is used to synchronize the reception of two sets of multiple-bit data values at the receiver circuit [Fig. 1; col. 3, lines 45-50].

20. As per claim 10, Cassiday et al teach that for each group, the clock signal is used to synchronize the reception of two sets of encoded multple-bit data values at the receiver circuit Fig. 1, col. 3, lines 45-63; col. 4, lines 1-10], and wherein the second module includes for each group: a data decoder adapted to decode the multiple-bit data values [Fig. 1; inherent to the receiver], and a FIFO buffer adapted to store the decoded data [Fig. 4; RCV BUFFER 82; col. 11, line 17; a receive buffer circuit 82].

21. As per claim 11, Cassiday et al teach that for each group, the data decoder converts an 8-bit value to a 6-bit value [inherent to the characteristic of a decoder], and wherein the 6-bit value is stored in the FIFO buffer [Fig. 4; RCV BUFFER 82; col. 11, line 17; a receive buffer circuit 82].

22. As per claim 12, Cassiday et al teach that the second module further includes data processing circuitry [Fig. 4; receiver processing circuitry] and another FIFO buffer [Fig. 4; RCV BUFFER 82; col. 11, line 17; a receive buffer circuit 82].

23. As per claim 13, Cassiday et al teach that the second module is further adapted to align data [Fig. 1; Fig. 4].

24. As per claim 16, Cassiday et al teach

a parallel bus having parallel bus lines adapted to transfer digital data, the parallel bus lines being arranged in a plurality of groups wherein each group includes a plurality of data-carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried over the plurality of data-carrying lines of the group [Fig. 1; col. 3, lines 45-63];

a first module including data processing circuitry [Fig. 1; col. 3, lines 45-63; col. 6, lines 47-50; transmitter module; Fig. 3]; and

a second module including data processing circuit [Fig. 1; col. 3, lines 45-50; col. 4, lines 1-10, 25-27, 33-37; receiver module; Fig. 4].

25. As per claim 17, Cassiday et al teach that the first module and second module include respective circuitries for processing data [Fig. 3; Fig. 4].

26. As per claim 18, Cassiday et al teach that for each group, the clock signal is differential and is used to synchronize [Fig. 1; col. 8, lines 13-14; differential signal wires LINK(1) and LINK(0) connecting each transmitter circuit to each receiver circuit].

27. As per claim 19, Cassiday et al teach that the second module is further adapted to align the data [Fig. 1; Fig. 4].

28. As per claim 20, Cassiday et al teach

a parallel bus having parallel bus lines adapted to transfer digital data, the parallel bus lines being arranged in a plurality of groups wherein each group includes a plurality of data carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried over the plurality of data-carrying lines of the group [Fig. 1; col. 3, lines 45-63];

first means for transferring sets of data concurrently on the plurality of groups of lines of the parallel bus [Fig. 1; col. 3, lines 45-63; col. 6, lines 47-50; transmitter module]; and

second means for collecting, for each group, the digital data carried from the first means over the plurality of data-carrying lines as synchronized by the clock signal for the group and for

align the data collected for each group and overcome any skew-caused misalignment between data concurrently transferred in different groups [Fig. 1; col. 3, lines 45-50; col. 4, lines 1-10, 25-27, 33-37; receiver module].

29. As per claim 21, Cassiday et al teach a method transferring digital data from a first module to a second module over a parallel bus having parallel bus lines susceptible to skewing data carried by the bus [Fig. 1], the method comprising:

arranging the parallel bus lines in a plurality of groups, each of the groups including a plurality of data-carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried from the first module to the second module over the plurality of data-carrying lines of the group [Fig. 1; col. 3, lines 45-63];

transferring sets of data concurrently using the groups of lines of the parallel bus [Fig. 1; col. 3, lines 45-63; col. 6, lines 47-50; transmitter module]; and

at the second module and for each group, collecting the digital data carried from the first module over the plurality of data-carrying lines as synchronized by the clock signal for the group [Fig. 1; col. 3, lines 45-50; col. 4, lines 1-10, 25-27, 33-37; receiver module]; and

at the second module, aligning the data collected for each group and overcoming any skew-caused misalignments between data concurrently transferred in different groups [Fig. 1; col. 3, lines 45-50; col. 4, lines 1-10, 25-27, 33-37; receiver module].

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 14 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Cassiday et al (US Patent no 5,978,419) in view of Manjunath et al (US Patent no 6,324,503 B1).

32. As per claim 14, Cassiday et al disclose the invention substantially. Cassiday et al do not disclose expressly about having a feedback communication path adapted to feed information from the second module to the first module. However, Manjunath et al clearly disclose about a feedback loop from receiver to transmitter [Fig. 7; col. 8, lines 42-51]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to data transfer from transmitter to receiver. Moreover, as

Manjunath et al expressly disclose the invention in light of improving the performance of data transfer. A routineer in the art would easily realize the benefit of having a feedback and will use the same technique to warn the transmitter in other cases as required, such as, near-full condition of buffer.

33. As per claim 15, Cassiday et al disclose the invention substantially. Cassiday et al do not disclose expressly about having the first and second modules being reciprocal. However, Manjunath et al clearly disclose about a transmitter and receiver modules being reciprocal [Fig. 7; col. 8, lines 42-51]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to data transfer from transmitter to receiver. Moreover, a routineer in the art would easily realize the benefit of having a transmitter and receiver modules talking back and forth as this will eliminate extra circuitry creation for just doing backward communication.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
April 27, 2004

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